Please add the following claims:

--21. A computer readable medium comprising instructions for a computer implemented chip design method, said method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints; and

e) checking said wired integrated circuit.

22. The computer readable medium comprising instructions as recited claim 21, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

23. The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including a connection to power rail or to a power return rail.

24. The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including an ESD